

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Attila Kovacs  
Assignee: NEC Electronics America, Inc  
Title: SYSTEM AND METHOD FOR REDUCING TIMING  
VIOLATIONS DUE TO CROSSTALK IN AN INTEGRATED  
CIRCUIT DESIGN  
Serial No.: Unassigned Filing Date: Herewith  
Examiner: Unassigned Group Art Unit: Unassigned  
Docket No.: NEC0255US

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Austin, Texas

MAIL STOP PATENT APPLICATION  
COMMISSIONER FOR PATENTS  
P. O. BOX 1450  
ALEXANDRIA, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**  
**37 CFR § 1.97(b)**

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying PTO Form-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

**EXPRESS MAIL NUMBER:**

**EV 304737412 US**

Respectfully submitted,



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Attorney for Applicant(s)  
Reg. No. 48,509

U.S. Department of Commerce, Patent and Trademark Office						Atty Docket No.		Serial No.	
						NEC0255US		Unassigned	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT						Applicant(s)			
(Use several sheets if necessary)						Attila Kovacs			
						Filing Date		Group	
						Herewith		Unassigned	
U.S. Patent Documents									
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
	AA								
	AB								
Foreign Patent Documents									
							Translation		
		Document	Date	Country	Class	Subclass	Yes	No	
	AC								
	AD								
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)									
	AE	Yasuhiko Sasaki and Naoki Kato, "Electronic Circuit Device and its Design Method", filed August 7, 2001; Serial No. 09/922,747, Publication No. US 2002/0104064 A1, Publication Date August 1, 2002.							
	AF	Albert E. Casavant, "Crosstalk Mitigation Method and System", filed October 16, 2001; Serial No. 09/977,372, Publication No. US 2002/0166101 A1, Publication Date November 7, 2002.							
	AG	Magma Design Automation, Inc., "Blast Noise," <a href="http://www.magma-da.com/c/@5W5T6bRF5RBy./Pages/blastnoise.html">http://www.magma-da.com/c/@5W5T6bRF5RBy./Pages/blastnoise.html</a> , 2002, pp. 1-2.							
	AH	Murat Becer, et al., <i>Motorola, Inc.</i> , "Signal Integrity Management in an SoC Physical Design Flow," ISPD'03, April 6-9, 2003, pp. 39-46.							
	AI	Richard Goering, <i>Planet Analog</i> , "Motorola Designers Offer Ways to Check IC Noise," <a href="http://www.planetanalog.com/showArticle?articleID=12803998">http://www.planetanalog.com/showArticle?articleID=12803998</a> , April 11, 2003, pp.1-2.							
	AJ	EE Times, "How Crosstalk Causes Problems," <a href="http://www.eedesign.com/story/OEG20020604S0046">http://www.eedesign.com/story/OEG20020604S0046</a> , June 5, 2002, pp. 1-2 (printed August 26, 2003).							
	AK	Tak Young, <i>Monterey Design Systems, Inc. and EE Times</i> , "IC Layout Must Avoid Crosstalk Problems," <a href="http://www.eedesign.com/story/OEG20020604S0045">http://www.eedesign.com/story/OEG20020604S0045</a> , June 5, 2002, pp. 1-4 (printed August 26, 2003).							
	AL	Bijan Kiani and Anthony Hill, <i>EE Times, Synopsys, Inc and, Texas Instruments, Inc.</i> , "Static Crosswalk Analysis Assures Silicon Success," <a href="http://www.eedesign.com/story/OEG20020604S0047">http://www.eedesign.com/story/OEG20020604S0047</a> , June 5, 2002, pp. 1-4 (printed August 26, 2003).							
	AM	ASIC News, "Cadence Introduces CeltIC 4.0," <a href="http://www.chipcenter.com/asic/products_300-399/prod300.html">http://www.chipcenter.com/asic/products_300-399/prod300.html</a> , pp. 1-4 (printed August 26, 2003).							
Examiner			Date Considered						
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.									